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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,571	01/23/2004	Khader S. Abdel-Hafez	3380-Z	3030

7590 11/18/2005

Law Office of Jim Zeggeer
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EXAMINER	
DILDINE JR, R STEPHEN	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,571	ABDEL-HAFEZ ET AL.	
	Examiner	Art Unit	
	R. Stephen Dildine	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-89* is/are pending in the application.

4a) Of the above claim(s) *34-49 and 67-89* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7,8,19,21-23,33,50,53,60,62,64 and 66* is/are rejected.

7)☒ Claim(s) *2,3,6,9-18,20,24-32,51,52,54-59,61,63,65 and 75-79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 34-49 and 67-89 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 3 November 2005.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 7-8, 19, 21-23, 33, 50, 53, 60, 62, 64 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al. (6,557,129) and further in view of Wang et al. (2002/0120896). Rajski shows a method and apparatus for selectively masking selected scan cells in an integrated circuit having plural scan chains (Figure 8), plural pattern generators (Column 10, lines 55-56 of Rajski), output-mask controller (Column 5, lines 43-44), and an output-mask network (Figure 8), comprising a means (or step) for (a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation (Column 10, line 55 of Rajski); (b) capturing a test response to all said scan cells during a selected capture operation (Column 9, lines 27-28 of Rajski); (c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation (Column 7, lines 10-12 of Rajski); and (d) repeating steps (b) to (c) until a predetermined limiting criteria is reached (Claim 67 of Rajski recites plural loading and storing steps for example). Rajski fails to disclose a plurality of pattern compactors, however Wang et al. discloses, that in a circuit testing system having plural scan chains, it is well known to provide plural pattern compactors (217, 218, 219 in Figure 2 of Wang) along with plural stimuli (pattern) generators. Figure 1 of Rajski et al. shows that the recitations of claim 4 are known in the prior art (see 14). Applicants' claim 7 is shown by Rajski et al. at control logic 152 (Figure 12). As for applicants' claims 8, 23 and 64, Rajski states (Column 8, lines 18-25) "At the appropriate time, an update line 165 is activated to move the data from the shift register to a control register 169. Each bit position that is activated in the

control register 169 allows a test response from the scan chains 164 to pass to the compactor. All other test responses are masked. Thus, the selective compactor can mask any variable number of test responses." Rajski et al. discloses (Figure 8, selector circuit 46 for example) the output-mask network comprises AND, OR, NAND or NOR gates as in applicants' claims 19, 33, 60 and 66.

Claims 2-3, 5-6, 9-18, 20, 24-32, 51-52, 54-59, 61, 63, 65 and 75-79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chu et al. (6,901,546) and Hapke (JP 2002-122639) are cited to show scanning with masking, Vranken et al. (WO 2005031378) is cited to show a masking circuit coupled between a circuit under test and a compactor, Adusumilli et al. (6,543,018) is cited to show NAND components used in scan test masking, Wang et al. (2003/0154433) is cited to show a mask network including AND gates, Rajski et al. (2004/0230884) is cited to show compacting, the article by Liu et al. is cited to show partitioning scan cells and the article by Huang et al. is cited to show locating faulty scan chains.

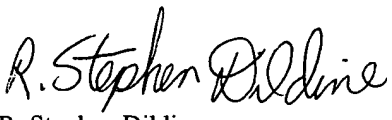
The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-3, 5-6, 9-18, 20, 24-32, 51-52, 54-59, 61, 63, 65 and 75-79 are allowable because the cited prior art does not teach or fairly suggest generating a compressed stimulus (claims 2-3, 51-52), presetting the output-mask controller (claims 6, 55 and 63), plural sequential-mask signals (claims 9-18), plural selected pattern-mask controllers (claims 24-32), selectively forcing selected constant logic values into all the scan cells (claims 56-59, 63), where there is a selector means to select between MISR or linear compactor (claims 20 and 61) or where there is a selector means to select between a SR or a range decoder (claim 65) or transforming said sequential circuit model into an equivalent combinational circuit model (claims 70-79) or an PRPG or RPG selectively (claims 5 and 54).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is (571) 272-3820. The examiner can normally be reached on M - F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



R. Stephen Dildine

R. Stephen Dildine
Primary Examiner
Art Unit 2133